laser annealing the amorphous semiconductor material to form a single crystalline semiconductor layer containing germanium;

doping the single crystalline semiconductor layer and the substrate at a source location and a drain location to form a source region and a drain region, whereby a channel region between the source region and the drain region includes a thin semiconductor germanium region; and

siliciding the source region and the drain region to form a silicide layer, the silicide layer extending into the substrate.

11. (Thrice Amended) The method of claim 1, further comprising:

providing a second amorphous semiconductor material above the amorphous semiconductor material including germanium after the laser annealing step;

performing another laser annealing step to form a second single crystalline semiconductive layer from the second amorphous semiconductor material; and

wherein the siliciding step forms the silicide layer so that the depth of the silicided layer is deeper than the second single crystalline semiconductor layer.

12. (Twice Amended) A method of manufacturing an ultra-large scale integrated circuit including a transistor, the method comprising steps of:

depositing an amorphous silicon germanium material above a top surface of a semiconductor substrate;

first annealing the amorphous silicon germanium material;

depositing an amorphous silicon material above the silicon germanium material;

second annealing the amorphous silicon material; and

providing a source region and a drain region for the transistor, the source region and the drain region being deeper than a combined thickness of the silicon germanium material and the silicon material.

Please add new Claim 29

29. (New)The method of claim 12 further comprising:

siliciding the source and the drain region to form a silicide layer, wherein the silicide layer extends deeper than the combined thickness.